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An Improved Bandgap Reference (BGR) Circuit with Constant Voltage and Current Outputs

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Abstract

Bandgap Reference (BGR) circuit is the main crucial element in designing any electronic systems. It has a stabilized voltage/current value over process-voltage-temperature (PVT) variations. In this paper, an enhanced 2-stage BGR circuit with constant voltage and current outputs is presented with a 1.2 V supply voltage. The first stage provides a fixed BGR voltage of 1 V with a temperature coefficient (TC) of 35 ppm/^{0}C. It includes a 2-stage op-amp for higher power supply rejection ration (PSRR). The op-amp has a closed feedback loop to neglect the current proportional-to-absolute-temperature (PTAT) and the negative TC. The second stage provides a higher current gain and an enhanced PSRR. It produces a fixed BGR current of 100 µA. Simulation results including PVT variations and Monte Carlo analysis have been performed, in 65 nm CMOS technology, to the proposed design which achieves a chip area of 0.03 mm^2, a higher temperature range of -80~120^{0}C, a 35 ppm/^{0}C TC, a -32 dB PSRR at 0.1 MHz and a 0.13 µW consumed power

Keywords: Bandgap Reference (BDR), Temperature coefficient, Constant Voltage.

1. Introduction

Nowadays, fixed Bandgap Reference (BGR) voltage and current circuits become the most commonly used and crucial blocks in designing various analog/mixed electronic subsystems. The reference circuit is called a bandgap as the silicon gap band is near to its reference voltage [1]. The main objective behind BGR circuits is to have a stabilized precision of the reference voltage/current over process-voltage-temperature (PVT) variations. Hence, there is no need for a calibration circuit for the BGR circuit to compensate these variations. Consequently, a PVT independent BGR circuit proposes a high accuracy electronic system.

The capacity of demands in integrated circuits has increased for the need of accurate references that exploit the common physical properties of such analog devices (i.e. MOSFETs, BJTs and diodes) [1]. Under certain bias conditions, these devices are able to produce accurate constant voltage/current outputs.

The conventional BGR circuits are not suitable for modern technologies, as they could not have a lower supply voltage than 1.5 V, for several reasons [2]–[4]. The temperature coefficient (TC) of the BJT base-emitter voltage is temperature-dependent as in equation (1); whereas V_{BG}, V_{BE}, V_{Th}, E_g, q, m are the bandgap reference voltage, the BJT base emitter voltage, the threshold voltage, silicon gap band energy, electron charge and a constant, respectively. This creates an error if the positive TC quantity exhibits a constant coefficient. Moreover, it is hardly to access npn-type BJTs for such conventional BGRs in CMOS technology. Although lateral pnp-type BJTs are suitable alternatives for npn type BJTs.

$$V_{BG} = \frac{V_{BE}-(4+m)\times V_{Th}+{E_g}/{q}}{T} \quad (1)$$

They have much lower current gain (β). In additions, the conventional BGR exhibiting operational amplifier (op-amp) circuit provides large DC offsets. This lets conventional BGR circuits have such a higher reference output of 1.25 V. This offset can be compensated by enlarging transistors sizes of the op-amps in the expense of large power and area.

At deep submicron CMOS technology scaling, the supply voltage decreases. This arises the need up to involve a low-

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voltage BGR circuit in lower technology node systems such as a proportional to absolute temperature (PTAT) based BGR [3]–[4], . Hence, conventional BGR circuits are no longer used. Although low-voltage BGR circuits have been introduced in the literature [1]–[4], they also face design complexity due to the analog characteristics degradation in deep submicron scaling. In fact, they do not get any such advantage of the CMOS scaling [3]. High speed op-amps suffer from much variations, in addition to larger power consumption. Moreover, the low-voltage BGR accuracy mostly depends on process-related parameters and on design matching techniques which could be performed by high-cost post-fabrication devices with dimensions larger than the lithographical minimum.

In this paper, a new 2-stage PVT-independent BGR circuit is introduced to provide fixed voltage and current outputs using 65 nm CMOS technology and a 1.2 supply voltage. Monte Carlo analysis is provided to model random mismatches between different components due to these process variation. The 1st stage of the proposed design is a constant 1-V bandgap reference circuit, with a voltage TC of 35 ppm/^{O}C, which has a closed feedback loop to neglect the effect between the current PTAT and the negative TC of the current.

The 2nd stage is a current reference circuit which produces a constant current of 100 µA. It is based on a class AB amplifier which takes the output of the BGR voltage circuit in order to provide a higher output current gain, a low output power and a better efficiency and linearity. Moreover, it enhances the system stability by splitting the output capacitance from the input one. Diodes are exhibited instead of lateral pnp-type BJTs as current digital semiconductor systems are based on CMOS technology.

The rest of the paper is organized as follows. The proposed design and the analytical analysis on the design operation are presented and discussed in Section II. Simulation results of the voltage/current outputs for the PVT variations are figured with

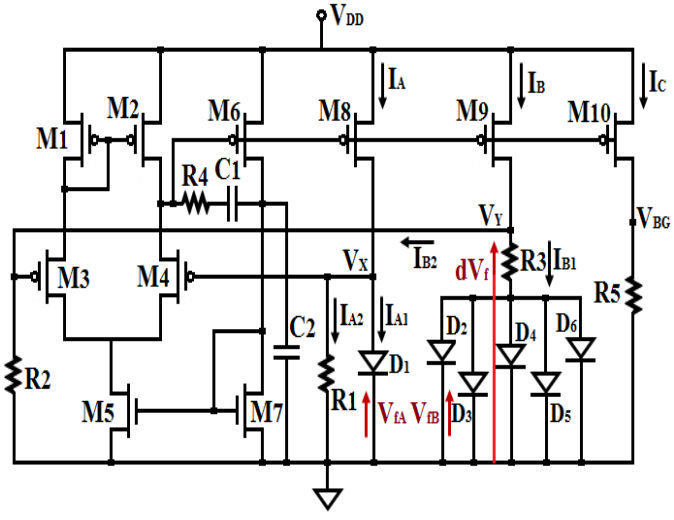

Fig. 1. Voltage reference circuit of the proposed design.

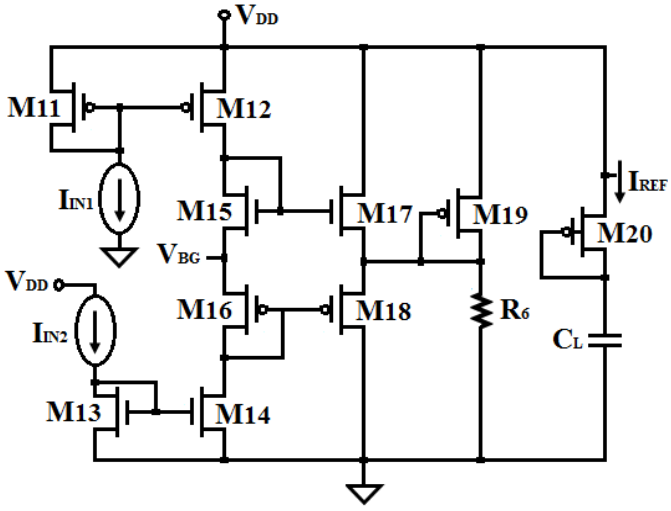

Fig. 2. Current reference circuit of the proposed design.

Monte Carlo analysis, illustrated and compared to various state-of-the-art BGR references in Section III. Finally, a summary is concluded in Section IV

2. Proposed Design and Analysis

In this work, 1-V constant voltage and 100 µA constant current references are proposed. Fig. 1 shows the voltage reference circuit schematic. The BGR voltage depends on both currents I_B and I_A which are produced by the closed feedback loop of V_Y and V_X, respectively. They are functions of: the thermal voltage (V_T) which equals to Boltezmann's constant multiplied by the room temperature and divided to the electron charge; and the diode voltage (V_f), respectively.

The constructed op-amp by M1-M7 is a 2-stage differential design in order to produce a larger gain, a higher output swing and to reject the common mode noise. In fact, the differential op-amp suits the low speed applications. It senses the difference between V_Y and V_X to get the current TC equation of I_A and I_B. Hence, both nodes V_Y and V_X are identical. The closed feedback loop ensures the drain voltages of M8 and M9 track the voltage diode of D1 (V_{fA}) which has a negative TC.

Capacitor C1 and resistance R4 provide 2 current paths so as to enhance the system stability and to make the phase margin (PM) become larger than 60^{O} (i.e. the system is stable) [4]. The first path, which forms a typical Miller compensation in a two-stage op-amp, establishes a dominant pole at the output of first stage (drain of M2 and M4). The second path produces a zero in the frequency domain. The constructed zero on the AC response is so near to the DC by making R4 shall equal to the inverse of the M6 trans-conductance (g_{m6}). Finally R4 is the nulling resistor used to ensure the stability occurs.

Currents I_A, I_B and I_C are identical due to the usage of the current mirror and as the resistance R1 equals to R2 and M8, M9 and M10 have the same sizes as well. Hence, these currents could track each other. As a result, I_{A1} equals to I_{B1}, while I_{A2} equals to I_{B2}. The voltage across R3 is the difference between the voltage diode D1 (V_{fA}) and the voltage diode D2 (V_{fB})

which is PTAT. Equation 2 shows the relation between I_{B1}, I_{B2} with V_{fA} and dV_f, respectively, which is the difference of the forward voltage among N numbers of diodes in the V_Y branch (D2-D6) and the D1 diode in the V_X branch. dV_f is also a function in the thermal voltage as in equation 3.

The inverse PTAT diode voltage and the PTAT voltage difference are converted into I_{B1} and I_{B2} and summed at the drain of M9 and mirrored to M10 to produce I_C. The final formula of the exact BGR voltage (V_{BG}) could be measured as in equation 4. The values of N, R1 and R2 are chosen to equate the positive and negative TCs. The drain-source voltage of M8, M9 and M10 should be reduced once their flowing current is reduced. This could be ascertained if these transistors operate on the saturation mode. Hence, the proposed reference voltage by the BGR circuit can also be minimized to the diode voltage level if the supply voltage is reduced to the same level. In other words, the scaling factor and R5 values are chosen to scale the reference value.

Class AB amplifier, shown in Fig. 2, constructed by M15- M18 transistors is considered a current gain output buffer circuit. Each transistor operates at the half of the applied input signal and the complementary transistors operate at the other half of the input signal. In other words, if V_{BG} is greater than the threshold voltage (V_{TH}), nMOS transistors (M15 and M17) are on and pMOS transistors (M16 and M18) are off. This makes the current flow from the upper current source constructed by M11-M12 and I_{IN1}. With the same method if V_{BG} is lower than V_{TH}, the pMOS transistors are on and nMOS transistors are off and the current flows from the lower current source constructed by M13-M14 and I_{IN2}. For this purpose, I_{IN1} and I_{IN2} should be transistors in deep saturation mode.

The region where both complementary transistors are nearly off (mid values of V_{BG}) is reduced. This results in minimizing the crossover when the signals of the M15 and M16 are combined. The feedback connection of M17 drain generates the necessary gate voltage for M19 transistor to track V_{BG} and to ensure that I_{REF} equals to V_{BG} multiplied by the M number and divided into R6. Whereas M is the float number to scale and enlarge the size of M20 transistor with respect to M19 to have a larger I_{REF}.

Table 1: Devices Parameters of the Proposed Design

Device	Value	Device	Value
M1, M2, M11	0.4 µm/ 0.06 µm	M12, M13	0.8 µm/ 0.06 µm
M3, M4	0.4 µm/ 0.08 µm	M14	1 µm/ 0.07 µm
M5	0.44 µm/ 0.07 µm	M15, M16	0.2 µm/ 0.06 µm
M6	16 µm/ 2 µm	M17, M18	23 µm/ 0.07 µm
M7	6.2 µm/ 1.5 µm	M19	0.62 µm/ 0.06 µm
M8, M9	0.5 µm/ 0.08 µm	M20	0.44 µm/ 0.06 µm
M10	0.4 µm/ 0.08 µm	D_1 - D_6	1.33 μm^2
R1, R2 (413 kΩ)	22 µm/ 700 µm	R6 (12 kΩ)	9 µm/ 80 µm
R3 (79 kΩ)	15 µm/ 150 µm	C1	0.3 pf
R4 (0.5 kΩ)	3 µm/ 20 µm	C2	0.08 pf
R5 (177 kΩ)	12 µm/ 300 µm	C_L	0.1 pf

$$I_{B1}, I_{B2} = \frac{dV_f}{R_3}, \frac{V_{fA}}{R_2} \quad (2)$$

$$dV_f = V_{fA} - V_{fB} = V_T \times \ln(N) \quad (3)$$

$$V_{BG} = \frac{R_5}{R_2} \times V_{fA} + \frac{R_5 \times V_T \times \ln(N)}{R_3} \quad (4)$$

By scaling the size of M20 transistor, any current can be mirrored to get an aimed reference current. One disadvantage reveals at wider range of V_{DD} across temperature and process, which is the gate-source voltage of M19 cannot equal to V_{DD}-V_{BG}. Table I illustrates the proposed design parameters

3. Simulation Results

All simulations results of the proposed design have been carried out, on Cadence Virtuoso, using industrial hardware-calibrated Taiwan Semiconductor Manufacturing Corporation (TSMC) 65 nm CMOS technology. The diode structure is easily implemented by the compatible CMOS process as in Fig. 3. The proposed design supply voltage is 1.2 V. All resistances used in the proposed design are transistor based.

To make sure that the system is stable, the AC analysis of the proposed design is checked. The output-input gain phase and magnitude are drawn versus the frequency domain as shown in Fig. 4(a) and Fig. 4(b), respectively. The PM is considered the difference between 180^O phase and the phase at which the frequency intersects with the 0 dB line in the magnitude graph. The proposed design gain is 40 dB. In other words, the frequency will intersect with the 0dB-line at -78 ^{O}, so the system is stable as the PM is about 102 ^{O}.

Fig. 5 shows the V_{BG} towards ±10 % supply voltage variations. At typical conditions, the reference voltage equals to 1 V. The worst case voltage error appears at a +10 % supply voltage variation. It equals to 1 %. As the supply voltage is decr-eased, some transistors may go outside the saturation region (i.e. off, triode or sub-threshold regions). But as transistors have been designed to be in deep saturation region, no such changes would appear in the devices' parameters. Fig. 6 shows the V_{BG} towards wide temperature variations ranged from -80 ^{O}C to 120 ^{O}C. The proposed design TC at typical conditions equals to 35 ppm/^{O}C. The worst case voltage error appears at -80 ^{O}C with 0.4 %.

On the other hand, Fig. 7 shows the behavior of the current reference towards the supply variations. At typical conditions, the reference current equals to 100 µA.

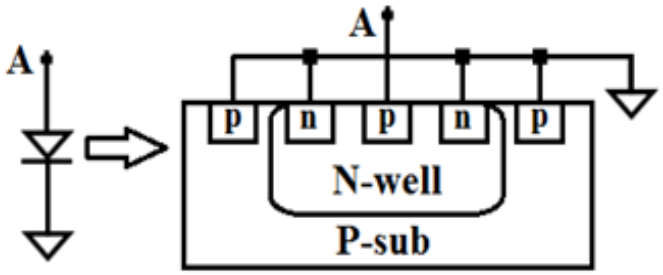

Fig. 3. Diode cross section design using a CMOS technology.

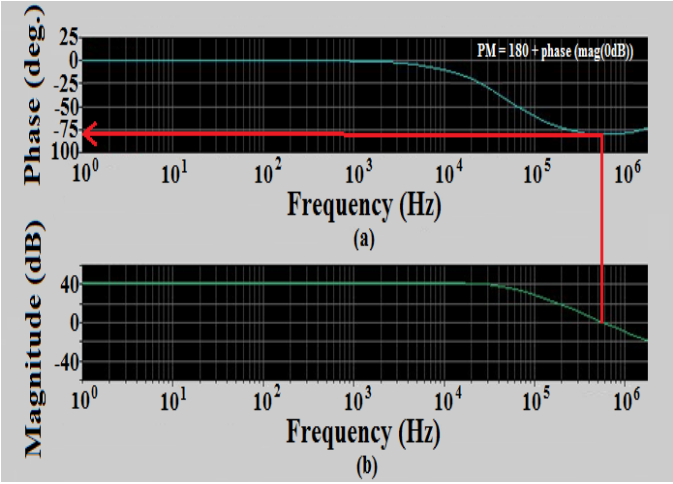

Fig. 4. AC analysis of the proposed design. (a) Phase vs. frequency graph. (b) Magnitude vs. frequency graph.

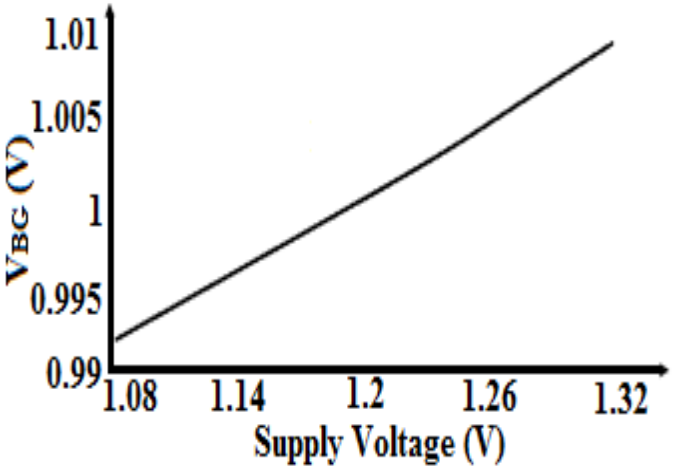

Fig. 5. The proposed design BGR voltage versus supply voltage variations.

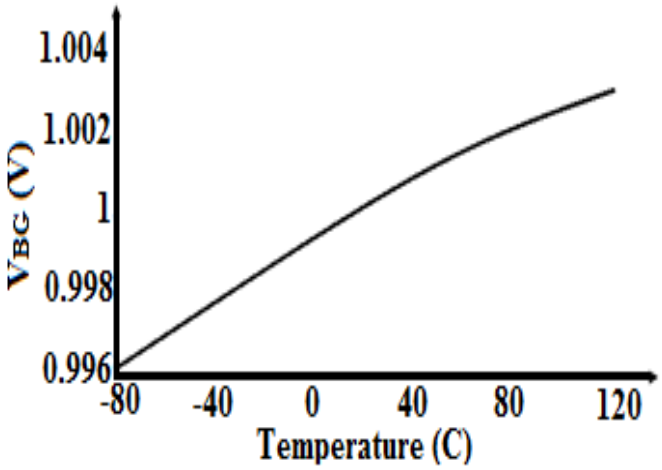

Fig. 6. The proposed design BGR voltage versus temperature variations at typical conditions.

The worst case current error appears at a +10 % supply voltage variation. It equals to 0.5 %. Fig. 8 shows the I_{REF} towards temperature variations. The worst case current error is considered to be 0.6 %.

The usage of the 2-stage op-amp and the class AB amplifier with current mirrors that include I_{IN1} and I_{IN2} is to increase the loop bandwidth in order to have an enhanced power-supply rejection ratio (PSRR). The PSRR of the proposed design is calculated from Fig. 5 at a frequency of 0.1 MHz. It equals to -32 dB. The consumed area of the proposed design equals to 0.03 mm^2, while the consumed power is 0.13 µW.

Due to CMOS technology scaling, process variations are expected to worsen in future technologies. They affect device parameters, resulting in fluctuations which change the reference voltage. The impact of these variations is typically evaluated by corner simulations. Process corners (SS corner which represents slow-speed nMOS and pMOS and FF corner which represents fast-speed nMOS and pMOS) have been simulated and compared to the typical-speed MOSFETs (TT corner).

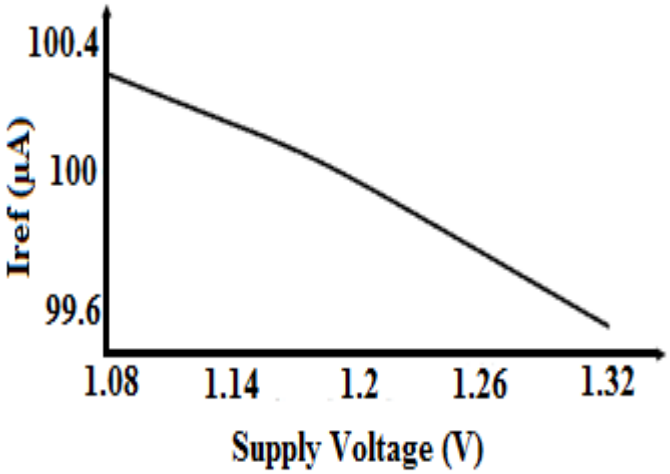

Fig. 7. The proposed design I_{REF} versus supply voltage variations.

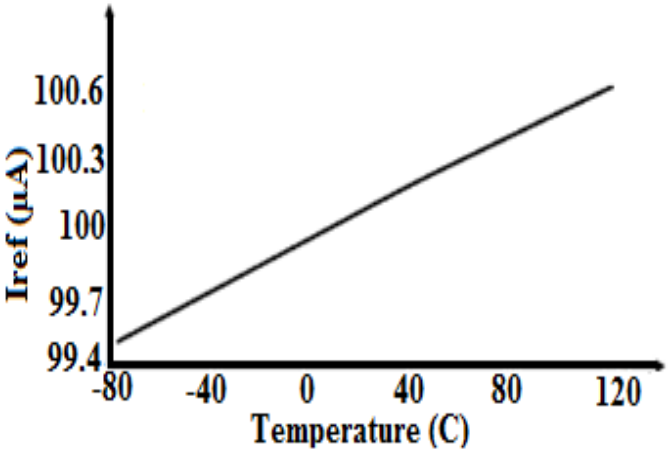

Fig. 8. The proposed design I_{REF} versus temperature variations.

Monte Carlo analysis has been performed from -80 ^{O}C to 120 ^{O}C temperature and at 10 KHz frequency to assess the proposed design robustness in case of process variations and devices' mismatches. Fig 9 shows that the mean BGR output error and the standard deviation over 1000 samples are around 0.83 mV, 105.4 mV respectively. The absolute worst case of the BGR voltage varies by less than 8 mV.

Table II represents both the BGR voltage and current values of the proposed design for the different corners at the minimum, typical and maximum temperature variations including Monte Carlo mismatches. The TC of the proposed design at the FF corner and the SS corner is 40 ppm/^{O}C and 32 ppm/^{O}C, respectively. The worst case voltage error of the FF corner and the SS corner appears at -80 ^{O}C with 0.38 % and at 120 ^{O}C with 0.32 %, respectively. Table III compares the proposed design with state-of-the-art bandgap reference circuits. From Table III This work provides a higher temperature range, a low chip area and reasonable temperature coefficient and PSRR.

Table 2: Typical BGR voltage and current values including Monte Carlo Mismatches at different corner and temperature variations

Parameter	Temperature Variations			TC
	-80^{0}C	27^{0}C	120^{0}C	(PPM/^{0}C)
V_{BG} @ SS (V)	0.9948	0.998	1.0012	32
V_{BG} @ SF (V)	0.995	0.9982	1.002	33
V_{BG} @ TT (V)	0.996	1	1.03	35
V_{BG} @ FS (V)	1.0336	1.03	1.041	37
V_{BG} @ FF (V)	1.046	1.05	1.054	40
I_{REF} @ SS (µA)	98.3	99	99.8	75
I_{REF} @ SF (µA)	100.08	99.4	100.1	68
I_{REF} @ TT (µA)	99.46	100	100.6	57
I_{REF} @ FS (µA)	101.39	101.2	101.4	50
I_{REF} @ FF (µA)	101.5	102	102.4	44

Table 3: Performance comparison of the state of the art BGR Circuits

Parameter	This	[2]	[3]	[4]
Process (nm)	65	180	130	180
Supply (V)	1.2	1.2	1.2	1
V_{BG} (V)	1	0.77	0.74	0.5
I_{REF} (µA)	100	36	120	4.7
Temperature range (^{0}C)	-80 ~120	-40 ~120	-40 ~120	-10 ~110
Area (mm^{2})	0.03	0.036	0.1	0.04
TC (PPM/^{0}C)	35	4.5	4.2	2.3
PSRR (dB)	-32 at 0.1MHz	-55 at 10KHz	-30 at 10KHz	-84 at 100Hz

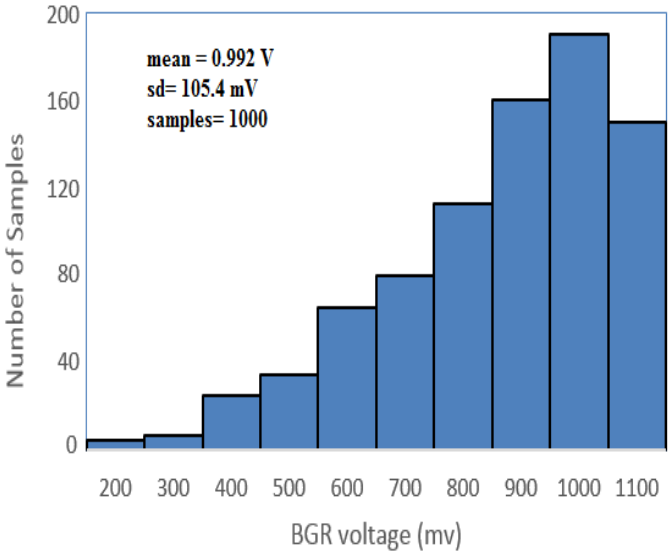

Fig. 9. Histogram of Monte Carlo simulation for BGR voltage.

4. Conclusion

In this paper, a novel 2-stage bandgap reference with constant voltage and current outputs are proposed. The 1st stage generates a fixed BGR voltage of 1 V with a TC of 35 ppm/^{O}C. It includes a 2-stage high-PSRR op-amp which has a closed feedback loop to track the aimed V_{BG} by neglecting the current PTAT and the negative TC. For usability in CMOS technology, diodes are used instead of the lateral pnp-type BJTs. The 2nd stage provides a fixed BGR current of 100 µA. It depends on class AB amplifier which provides higher current gain that also enhances the PSRR. Monte Carlo analysis and PVT variations have been simulated to show the design robustness. The proposed design achieves a low chip area, a higher temperature range and reasonable TC and PSRR. It can produce lower fixed current/ voltage with a low supply voltage by changing the output transistor scaling factor.

References

[1] G. Ge, C. Zhang, G. Hoogzaad, and K.A.A. Makinwa, "A Single-Trim CMOS Bandgap Reference With a 3£ Inaccuracy of ±0.15% From 40^{O}C to 125^{O}C," IEEE JSSC, vol. 46, no. 11, pp. 2693–2701, 2011.

[2] B. Ma, and F. Yu, "A Novel 1.2–V 4.5-ppm/°C Curvature-Compensated CMOS Bandgap Reference," IEEE TCAS I: Regular Papers, vol. 61, no. 4, pp. 1026–1035, 2014.

[3] Q. Duan, and J. Roh, "A 1.2-V 4.2-ppm/°C High-Order Curvature-Compensated CMOS Bandgap Reference," IEEE TCAS I: Regular Papers, vol. 62, no. 3, pp. 662–670, 2015.

[4] M.U. Abbasi, G. Raikos, R. Saraswat, and E. Rodriguez-Villegas, "A high PSRR, ultra-low power 1.2V curvature corrected Bandgap reference for wearable EEG application," 13th IEEE NEWCAS, pp. 1–4, 2015.